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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/042,733	10/25/2000	Curtis Priem	18659-15C1	8456

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EXAMINER

TUNG, KEE M

ART UNIT	PAPER NUMBER
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2676

DATE MAILED: 05/02/2003

5

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/042,733

Applicant(s)

PRIEM ET AL.

Examiner

Kee M Tung

Art Unit

2676

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 October 2000.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 13-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 13-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. The preliminary amendment filed 10/25/00 has been considered in preparing this Office action.

Drawings

2. The newly add drawing figure 2A and the respective areas of specification are **not entered** because it considers as containing subject matter, which was not described in the specification at the time the application, was filed (introduce new matter). Furthermore, the new drawing figure 2A labeled as "20" on the center of the page which is a cache memory and should be changed to --a graphics accelerator 15--.
- But, the figure and amendment to the specification are still considered as new matter.

Claim Rejections - 35 USC § 112

3. Claims 13-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 13, line 11, "a circuit" is not indefinite since it is clearly from the drawing and specification the circuit is the graphics accelerator and not a separate circuit from the graphics accelerator as claimed. Correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 13-16, 18, 19, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morgan et al (5,821,940).

As per claim 13, Morgan et al teaches a computer (Figs. 2 and 5) comprising a CPU (12); a bus (connecting between 14 and 16); a memory (14); and a graphics accelerator (combination of elements display list controller 16, transformation processor 18, cache storage means 22 and back end processor 24) coupled to the bus and including a cache (Fig. 5, 28) for data associated with vertices, the data of any of the vertices that is already resident in the cache can be used and reused to render any polygons defined by the vertices (col. 3, lines 30-43). It is noted that Morgan et al fails to explicitly suggest that the data for each of the vertices representing its respective attributes including its screen coordinates, color and a **fog** attribute and the circuit producing screen values for the respective attributes including a scaling circuit and a lighting pipeline. However, it would have been obvious to one of ordinary skill in the art at the time the present invention was made that the polygons are conventionally triangles (see figure 3 of Morgan et al) having vertices which are defined in world space by 3-D coordinates, color values, texture coordinates, fog values and other values as suggest by applicants (page 1, lines 9-22 of the instant specification) and the scaling circuit and a lighting pipeline are considered as part of the standard features or functions of any well known and well used graphics processor or accelerator or controller to one of ordinary skill in the art (see col. 1, line 29 for scaling) in order to

provide a high performance graphics processing system. Therefore, at least claim 13 would have been obvious.

As per claim 14, Morgan et al teaches the cache includes cache position for the data associated with the vertices the cache positions being indexed by an application program (Figs. 3 and 4 and col. 3, lines 44-63).

As per claim 15, Morgan et al teaches the cache has a memory mapped storage space for the data associated with the vertices of polygons (Figs. 3 and 4).

As per claim 16, Morgan et al teaches the cache includes cache position for the data associated with the vertices the cache positions being indexed by an address in a data structure of vertices in memory (Figs. 3 and 4).

Claim 18 is similar in scope to claim 13, and additionally requires providing indices for designating cache positions of data in a cache, the data being associated with vertices of any of the polygons (see figure 6, 28 and col. 4, lines 19-44); storing the data at the designated cache positions in the cache based on each of the indices being provided (cache memory 28); and issuing a command for rendering a polygon by indicating the indices for selecting the data associated with the vertices of the selected polygon (26).

As per claim 19, Morgan et al further teaches directing a CPU to transfer a command to a register (by display list controller 16).

As per claim 21, Morgan et al teaches creating an array of vertices in a memory and indexing data for each of the vertices which is stored in the array (by CPU 12, col.

Art Unit: 2676

3, lines 15-20) and selecting from the array vertices defining a polygon to be rendered (16) and transferring to the cache the data for each of the selected vertices (26).

Claim 23 is similar in scope to claim 13, and additionally requires a setup circuitry which would have been obvious by the teachings of transformation processor 18 of Morgan et al.

3. Claims 17, 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morgan et al (5,821,940) as applied to claims above, and further in view of Holt et al (5,760,792).

The teachings of Morgan et al are given in previous paragraph of this Office action. However, Morgan et al fails to explicitly teach a DMA engine for transferring the data to the cache. This is what Holt et al teaches. Holt et al a computer (Fig. 2) comprising a CPU (inherent, col. 2, lines 11-15 and col. 49-50); a bus (201); a memory (inherent, col. 2, line 50); and a graphics accelerator (Fig. 2, graphics processor board) joined to the bus including a DMA engine (211) for transferring data to a FIFO (21) for vertex data of polygons to be displayed. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of DMA engine of Holt et al into the system of Morgan et al in order to transfer vertex data from main memory to the graphics cache in high speed, such as, capable of burst transfer as taught by Holt et al (col. 2, lines 56-60). Therefore, at least claims 17, 22 and 24 would have been obvious.

Art Unit: 2676

4. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morgan et al (5,821,940) as applied to claims above, and further in view of Swanson (5,421,028).

The teachings of Morgan et al are given in previous paragraph of this Office action. However, Morgan et al fails to explicitly teach embedding the command in the data associated with the polygon. This is what Swanson teaches (col. 7, lines 10-29). Swanson further teaches the graphics transform engine 102 may perform tasks such as graphics context management, matrix transformation calculation, spline tessellation, and **lighting model computation** (col. 1, lines 52-55). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Swanson into the system of Morgan et al in order to a system whereby commands for pipelined processing circuits are passed into the pipeline along with the data and processed in the desired processing order as taught by Swanson (col. 1, lines 13-20). Therefore, at least claim 20 would have been obvious.

Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kee M Tung whose telephone number is 703-305-9660. The examiner can normally be reached on Tuesday - Friday from 6:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Art Unit: 2676

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-0377.

kmt
April 30, 2003



Kee M Tung
Primary Examiner
Art Unit 2676